IN THE CLAIMS:

Please amend the claims as follows.

1. (Currently Amended) A microprocessor comprising:

a plurality of execution units each configured to execute instructions;

an instruction dispatch circuit configured to dispatch said instructions for execution by said plurality of execution units;

a power management control unit coupled to said instruction dispatch circuit, wherein said power management unit includes a programmable unit for storing a particular value specifying a reduced power mode;

wherein said instruction dispatch circuit is configured to convey instructions to a restricted number of said plurality of execution units in response to said particular value being stored in said programmable unit;

a floating-point scheduler coupled to receive floating-point instructions dispatched from said instruction dispatcher;

at least one floating-point execution pipeline coupled to receive said floating-point instructions from said floating-point scheduler;

wherein said power management control unit is further configured to be programmed in a floating-point power reduced mode, wherein said floating-point scheduler is configured to stall dispatch of selected floating-point instructions to said at least one floating-point execution pipeline in response to said reduced floating-point power mode.

2. (Original) A microprocessor as recited in Claim 1 wherein said instruction dispatch circuit comprises an instruction alignment unit.

3. (Original) The microprocessor as recited in Claim 1 wherein each of said plurality of execution units is configured to execute integer instructions.

4. (Original) The microprocessor as recited in Claim 1 wherein each of said plurality of execution units is included within a corresponding execution pipeline.

5. (Original) The microprocessor as recited in Claim 4 wherein each corresponding execution pipeline includes a decode unit coupled to receive instructions from said instruction dispatch circuit and a reservation station coupled to receive a decoded instruction from said decoder.

6-8. Cancelled.

9. (Currently Amended) The microprocessor as recited in Claim ~~8~~ 1 wherein said power management control unit is configured to cause said floating-point scheduler to stall dispatch of selected floating-point instructions to said at least one floating-point execution pipeline during selected cycles.

10. (Currently Amended) A microprocessor comprising:

at least one execution unit configured to execute instructions;

an instruction dispatch circuit configured to dispatch said instructions for execution by said at least one execution unit;

a power management control unit coupled to said instruction dispatch circuit, wherein said power management unit includes a programmable unit for storing information corresponding to a reduced power mode;

wherein said instruction dispatch circuit is configured to stall dispatch of selected instructions to said at least one execution unit upon certain dispatch cycles in response to said information being stored in said programmable unit;

a floating-point scheduler coupled to receive floating-point instructions dispatched from said instruction dispatcher;

at least one floating-point execution pipeline coupled to receive said floating-point instructions from said floating-point scheduler;

wherein said power management control unit is further configured to be programmed in a floating-point power reduced mode, wherein said floating-point scheduler is configured to stall dispatch of selected floating-point instructions to said at least one floating-point execution pipeline in response to said reduced floating-point power mode.

11. (Original) The microprocessor as recited in Claim 10 wherein said at least one execution unit includes at least two execution units coupled in a parallel, superscalar configuration.

12. (Currently Amended) The microprocessor as recited in Claim ~~1~~ 10 wherein said programmable unit includes a counter containing a value that is modified upon each dispatch cycle, wherein a particular value of said counter controls the stall of said selected instructions.

13. (Original) A microprocessor as recited in Claim 10 wherein said instruction dispatch circuit comprises an instruction alignment unit.

14. (Original) The microprocessor as recited in Claim 10 wherein each of said plurality of execution units is configured to execute integer instructions.

15. (Original) The microprocessor as recited in Claim 10 wherein each of said plurality of execution units is included within a corresponding execution pipeline.

16. (Original) The microprocessor as recited in Claim 15 wherein each corresponding execution pipeline includes a decode unit coupled to receive instructions from said instruction dispatch circuit and a reservation station coupled to receive a decoded instruction from said decoder.

17-19. Cancelled.

20. (Currently Amended) The microprocessor as recited in Claim ~~19~~ 10 wherein said power management control unit is configured to cause said floating-point scheduler to stall dispatch of said selected floating-point instructions to said at least one floating-point execution pipeline during selected cycles.

21-23. Cancelled.